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Cu/LKD-5109 Damascene Integration Demonstration Using FF-02 Low-k Spin-on Hard-mask and Embedded Etch-stop

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Abstract

The feasibility of integrating low-k spin-on dielectrics into a Cu damascene structure using JSR's LKD-5109 (k=2.2) has been investigated. The chemical vapor deposited embedded etch-stop (ES) and dual hard-mask (HM) are replaced by JSR's spin-on dielectrics (organic FF-02 and MSQ type LKD-2022). In this study, the capability of FF-02 as an ES and as a chemical mechanical polishing (CMP) stop has been verified. In addition to electrical and mechanical film properties of FF-02, the chemical compatibility and removal rate to CMP slurries are investigated. Finally, the first successful single damascene (SD) integration with spin-on dual HM and ES is demonstrated and its electrical results including Raphael's model simulation of the k-value are reported.

Introduction

Reducing interline capacitance and line resistance is required to minimize RC delays and increasing power consumption in high-speed devices. For the 100 nm node and below, it will be essential to use Cu and low-k interlayer dielectrics (ILD) [1]. The use of low-k materials is important in decreasing the interline capacitance but the effect of HM and ES also needs to be considered while calculating the total capacitance. An effective dielectric constant (keff) can be defined, taking into account the contribution of all the dielectrics used. To decrease keff, it is becoming important not only to decrease the k-value of ILD but also to integrate HM and ES with lower k-value [2,3]. In this study, the conventional CVD HM and ES such as SiC with a k-value of 4.4 is replaced by low-k spin-on dielectrics. A successful spin-on dielectrics stack would facilitate integration procedures and reduce the cost of ownership, in addition to decreasing keff.

This paper presents an alternative scheme for a Cu damascene integration and its feasibility using LKD-5109 combined with low-k spin-on dielectrics, FF-02 (HM and ES) and LKD-2022 (sacrificial HM). FF-02 is a fully organic polyarylene based material, and both LKD-5109 and LKD-2022 are MSQ type materials. Prior to integration, film properties and CMP compatibility were investigated, particularly for FF-02. Finally, SD integration demonstration with spin-on dual HM and ES using a dual damascene (DD) stack (Fig.1(a)) was followed by electrical measurements.

Film characterization

A. Electrical and mechanical properties

Several blanket films with a 600 nm of LKD-5109 and LKD-2022 and with a 500 nm of FF-02 were coated on Si wafers with dynamic dispense in a TEL ACT8 SOD coater. Thereafter a soft bake step was performed at 200 °C for 1 minute. The films were then cured in a vertical furnace at 420 °C for 1 hour in N_2 atmosphere. Typical electrical and mechanical film properties were measured on these blanket wafers. Selected film properties are listed in Table1. A k-value of 3.3 was obtained for FF-02 using MIS capacitors.

Table 1 Selected film properties for low-k spin-on materials

	FF-02	LKD-5109	LKD-2022
T_R (up to 450C)[i]	None	None	None
Residual stress @RT(MPa)[i]	65	21	-
Dielectric constant[ii]	3.3	2.2	2.9
Refractive index @633nm[iii]	1.68	1.25	1.36
Leakage current @0.2MV/cm (A/cm^2)[iv]	2.0×10^{-11}	7.8×10^{-11}	-
Breakdown threshold(MV/cm)[iv]	2.6	4.3	-
Elastic modulus(GPa)[v]	5.0	4.9	14.1
Hardness(GPa)[v]	0.4	0.6	2.2

[i] Measured by thermal stress, [ii] Measured by MIS capacitors with Al dots at 100kHz, [iii] Measured with Ellipsometer, [iv] Measured by MIS capacitors with Hg dots, [v] Measured with nanoindentation

B. CMP compatibility

Chemical compatibility and removal rate against commercially available CMP slurries were investigated using blanket wafers for LKD-5109 and FF-02. The wafers were dipped into EKC MicroPlanar CMP 9011/9003 (barrier slurry), Cabot-SS-D7000 (buff slurry) and into Ashland OnTrak 2500 (cleaning solution), for 5 minutes at room temperature. FTIR and ellipsometric measurements

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PAGE 26/35 * RCVD AT 9/16/2005 8:43:45 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID:7709510933 * DURATION (mm-ss):10-48

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(a) DD spin-on dielectrics stack with patterned resist (b) SD structure after CMP

Fig.1 Stack details for single damascene integration with spin-on dual hard-mask and etch-stop.

were done on these wafers before and after the dip test. The results indicated that these chemicals did not affect LKD-5109 and FF-02.

Then, direct CMP was performed on the blanket wafers to evaluate their removal rates for the barrier and buff slurries. As a reference, a 90 nm thick TaN blanket film deposited by physical vapour deposition (PVD) and a 50 nm thick SiC blanket film deposited by CVD were included, which are conventionally used in integration for a barrier metal and a CVD HM, respectively. Film thickness before and after CMP process in Lam Teres was measured with KLA-Tencor UV1280. The results in Table 2 show that FF-02 has extremely low removal rates and its CMP stopping capabilities are at least as good as CVD-deposited SiC HM.

Table 2 Removal rate for blanket wafers

Slurry	Condition	RR (nm/min)			
		LKD-5109	TaN	SiC	FF-02
EKC MicroPlanar	2 psi/ 200rpm	92	95	6	≈0
Cabot-SS-D7000	1 psi/ 40rpm	138	16	1	≈0

Integration

A. Dual damascene stack and lithography

Clean Si wafers were coated with 50 nm Si_3N_4, 500 nm SiO_2 and 50 nm SiC, and on these materials the spin-on dielectrics were coated with via and trench level, as shown in Fig.1(a). A soft bake step was performed at 200 °C for 1 minute after each film deposition. First a 370 nm LKD-5109 for via level ILD and a 50 nm FF-02 ES was spin-coated. Consecutively, a 370 nm LKD-5109 for trench level ILD and a 150 nm FF-02 HM were spin-coated. After the wafers were cured at 420 °C for 10min on a DCC hotplate of a TEL ACT8 SOD coater, a 160nm LKD-2022 top HM was coated. Finally, the wafers were cured at 420 °C for 1hour in N_2 atmosphere in a vertical furnace. After completion of the stacks, no delamination was observed by scotch tape pealing test. However, further optimization of film deposition and cure steps is ongoing to remove failure risks such as delamination and crack generation in spin-on multi layer stack (more than 2 metal layers).

The TIS-2000 bi-layer resist system was used for trench lithography. The lithography was performed at 248 nm with 0.25 µm as the target value for the trench width.

B. Single damascene demonstration

SD integration was demonstrated on the full spin-on dielectrics stack. LKD-2022 top HM was opened in C_4F_8 chemistry, and then FF-02 HM was etched during resist removal in N_2/O_2 chemistry in LAM etch tools. Thereafter, the trench pattern of FF-02 HM was transferred to FF-02 ES in C_4F_8 chemistry. At the same time, LKD-2022 top HM was completely removed. No micro loading effect was observed in the trenches wider than 0.2µm. During the etch process, it was verified that FF-02 can be an excellent ES with an etch selectivity of >14 to LKD-5109.

After the etching process, a degassing step was done at 350°C for 3 minutes for desorbing the moisture. Then, a 25 nm SIP PVD TaN and a 150 nm SIP PVD Cu seed deposition were done, followed by a 1 µm Cu plating step. For the Cu/TaN CMP, a 3-step process was preformed using Cabot iCue 5001 for Cu removal, and the barrier and buff slurries listed in Table 2 (See Fig.1 (b)).

Finally, micro structural analysis was done after completion of integration. SEM observation for a 0.2 µm line/space structure after CMP is shown in Fig.2. The picture indicates good etch profile. Also the etch stop has not been punched through, indicating that FF-02 is a successful etch stop.

C. Electrical evaluation

Isolated Cu lines of 300 µm length with line widths ranging from 0.2 to 0.4 µm were evaluated by 4-point resistance measurements. Probability distributions of sheet resistances extracted from the actual Cu line dimensions are shown in Fig.3. Low sheet resistance and narrow distribution between 0.05 and 0.057 Ω/sq was obtained even for 0.2 µm wide lines. This indicates the robustness of the processing steps.

Meander-fork structures with lengths between 11 and 23 mm and line widths between 0.2 and 0.4µm were evaluated, and probability distributions of the sheet resistances are

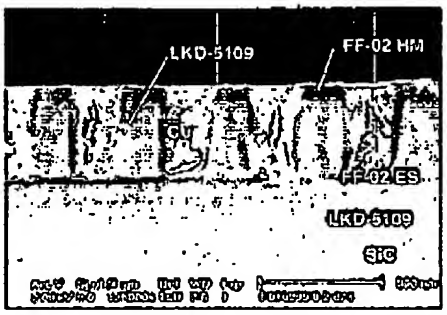

Fig.2 SEM cross-section for a 0.2µm line/space structure in spin-on dielectrics stack after CMP

PAGE 27/35 * RCVD AT 9/16/2005 8:43:45 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID:7709510933 * DURATION (mm-ss):10-48

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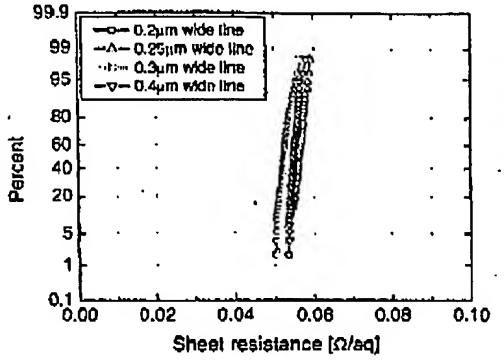

Fig.3 4-point resistance measurements for 300µm long isolated lines with line widths ranging from 0.2 and 0.4µm.

shown in Fig. 4. For 0.2 µm wide meanders, very few fall-outs can be seen and the variation within the wafer is small, indicating that the process is well optimised and FF-02 is a good CMP stop in particular.

keff-value was extracted for 0.175 to 0.4µm equal line/space structures by a TMA Raphael's model simulation. A 3-lines model including a 50nm CVD SiC cap with k=4.4 was created as shown in Fig.5. The plugged-in values for a thickness of LKD-5109 at via and trench level, and of FF-02 HM and ES were calibrated by SEM and FIB cross-sections of the experimental SD structures. k-values of 2.2 and 3.3 were used for LKD-5109 and FF-02, respectively. The results are shown in Table3 as compared to the case that CVD SiC was used for HM and ES in place of FF-02. About 7 % decrease of keff can be obtained for 0.2µm actual line/space structure.

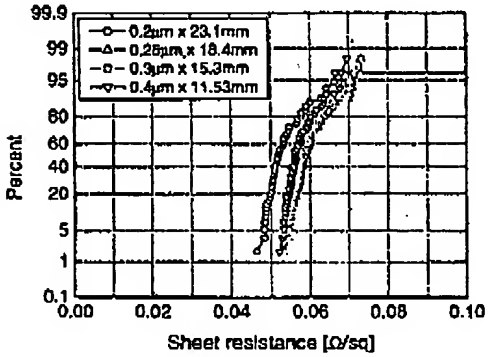

Fig.4 Continuity measurements of meander-fork structures with line widths ranging from 0.2 to 0.4µm.

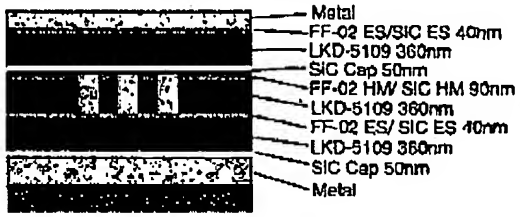

Fig.5 3-lines model created for keff simulation in dense line/space structures.

Table 3 Extracted keff-values for dense line/space structures

Material of HM / ES	keff for line/space (µm)				
	0.175	0.2	0.25	0.3	0.4
FF-02	2.58	2.57	2.56	2.55	2.53
SiC	2.78	2.77	2.74	2.72	2.67

Conclusion

The feasibility of integrating organic FF-02 spin-on dielectric into a Cu/LKD-5109 damascene structure as a HM and as an ES has been evaluated. FF-02 is chemically compatible to CMP slurries and proved to be an efficient CMP stop and embedded ES. The first successful SD integration has been demonstrated and good electrical results are obtained. Raphael's model simulation proves that, by using FF-02 HM and ES, keff-value is lowered by about 7 % in actual dense line/space structures, as compared to CVD SiC HM and ES.

Acknowledgements

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PAGE 28/35 * RCVD AT 9/16/2005 8:43:45 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID:7709510933 * DURATION (mm-ss):10-48